400Gb/s QSFP-DD DR4+ 2km SMF Transceiver

LA-OT-400G-DR4+-2M

General Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP-DD MSA-compliant edge type connector.

The product is designed with form factor, optical/electrical connection, and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity, and EMI interference.

Functional Description

The module incorporates 4 parallel channels on 1310nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver together with 4 parallel EMLs. On the receiver path, a PD array relates to a quad channel TIA to convert the parallel 400Gb/s optical input into 4 channels of parallel 100Gb/s (PAM4) electrical signals. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP-DD MSA with MPO-12 connector. A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with

the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Features

- QSFP-DD MSA compliant
- Parallel 4 Optical Lanes
- 100G Lambda MSA 400G-DR4 Specification compliant
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0 to 70°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel.
- Maximum power consumption 12W
- MPO-12 connector
- RoHS compliant

Applications

- 400G Ethernet
- Infiniband interconnects
- Enterprise networking

Transceiver Block Diagram

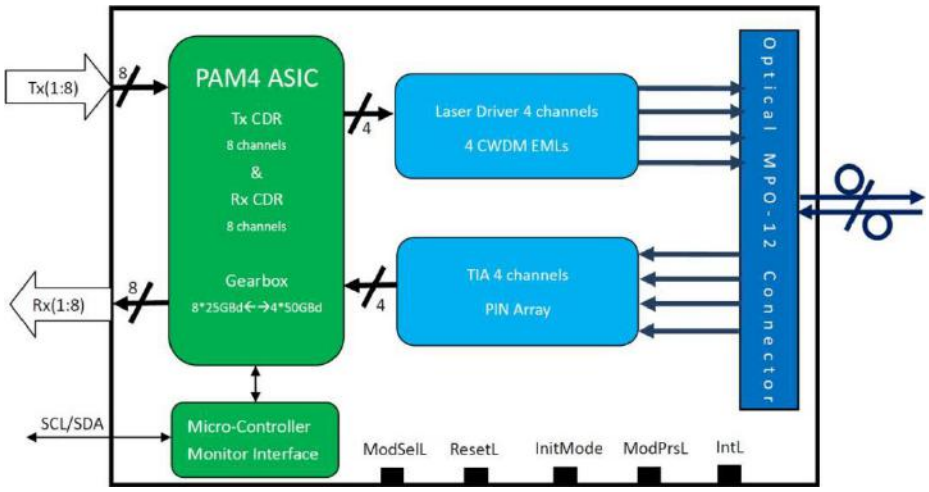


Figure 1. Transceiver Block Diagram

Pin Assignment and Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

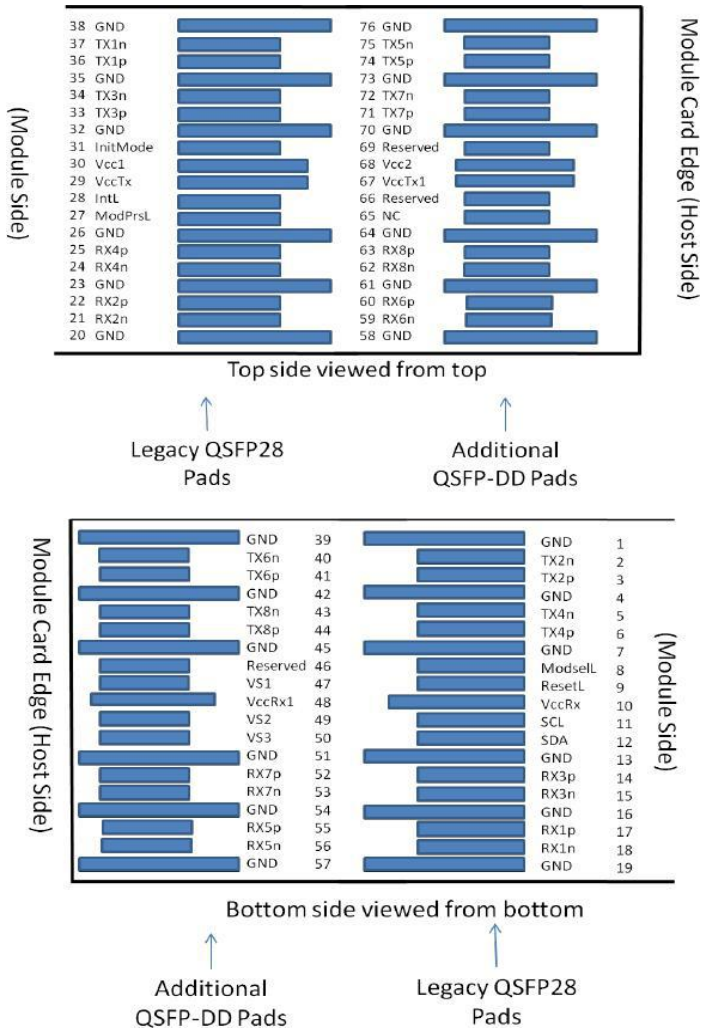


Figure 2. MSA Compliant Connector

Pin Definition

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted DataInput	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16	GND	Ground	1B		1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad iscalled LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	

38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted DataInput	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted DataInput	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Recommended Power Supply Filter

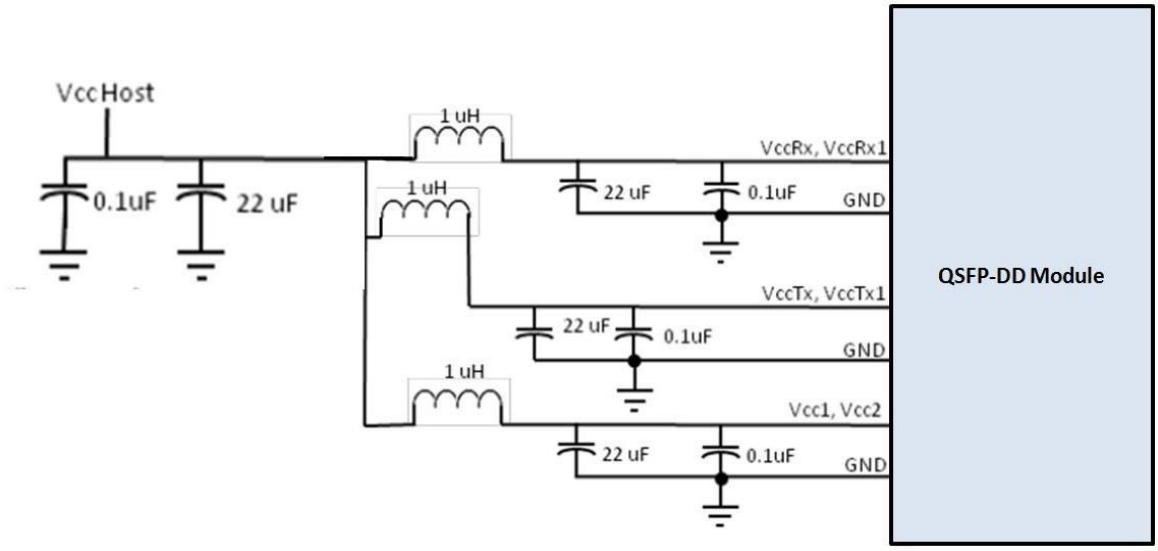


Figure 3. Recommended Power Supply Filter

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Case Temperature	T_{OP}	0	70	°C	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d	5.5		dBm	

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.002		2	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended OperatingEnvironment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk InputVoltage Tolerance	TP1a	900			mVpp	1
Differential TerminationMismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to CommonMode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential TerminationMismatch	TP4			10	%	
Differential Output ReturnLoss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye SymmetryMask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height,Differential	TP4	70			mV	
Far-end Eye Symmetry MaskWidth (ESMW)	TP4		0.2		UI	
Far-end Eye Height,Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode OutputVoltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q orscrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3.DC common mode voltage generated by the host. Specification includes effects ofground offset voltage.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	P_{AVG}	-2.4		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.2		4.2	dBm	2
Launch Power in OMA_{outer} minusTDECQ, each Lane for ER ≥ 4.5dB for ER < 4.5dB		 -1.6 -1.5			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
TDECQ – 10*$\log_{10}(C_{eq})$, each Lane				3.4	dB	3
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	dB	
$RIN_{17.1}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFFTransmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Damage Threshold, each Lane	TH_d	5.5			dBm	4
Average Receive Power, each Lane		-6.4		4.5	dBm	5
Receive Power (OMA_{outer}), each Lane				4.7	dBm	
Receiver Sensitivity (OMA_{outer}),each Lane	SEN			Equation(1)	dBm	6
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-2.5	dBm	7
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9.4	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 8)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
SECQ – 10*$\log_{10}(C_{eq})$, Lane underTest				3.4	dB	
OMA_{outer} of each Aggressor Lane			4.7		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant;however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for anextinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts forreference equalizer noise enhancement.
4. Average receive power, each lane (min) is informative and not the principal indicator ofsignal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 4.

$$RS = \max(-4.5,\ SECQ - 5.9)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.
8. These test conditions are for measuring stressed receiver sensitivity. They are notcharacteristics of the receiver.

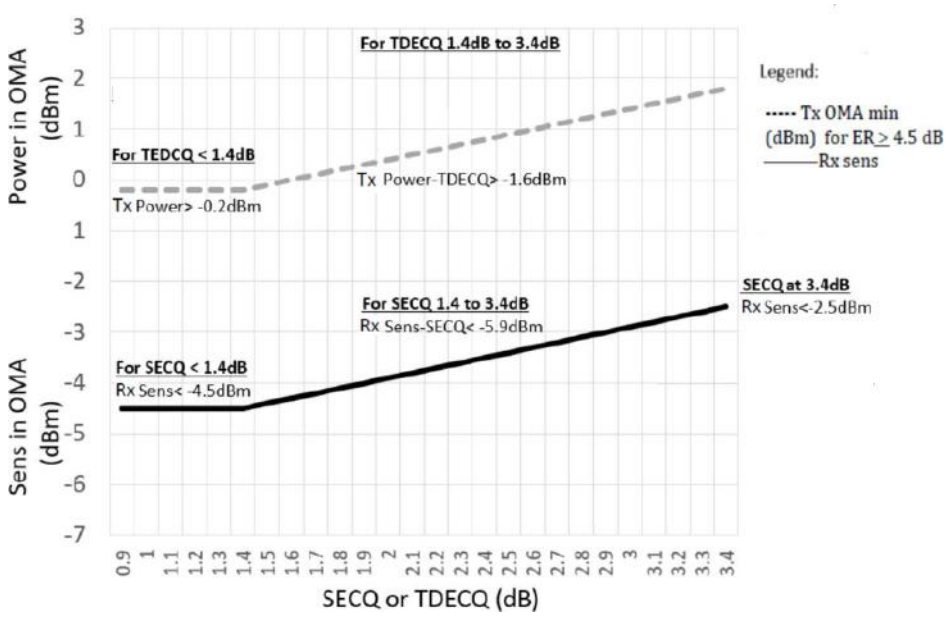


Figure 4. Illustration of Receiver Sensitivity Mask for 400G-DR4+

Digital Diagnostic Functions

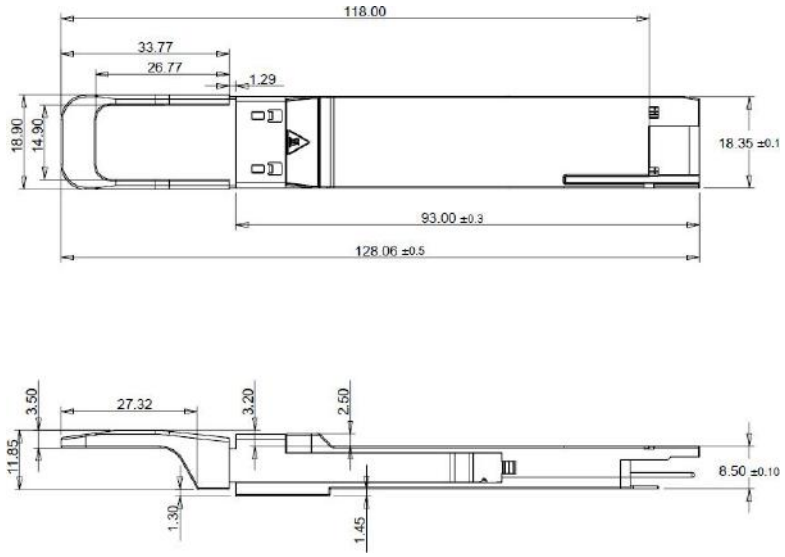
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature MonitorAbsolute Error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power MonitorAbsolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Outline Drawing (mm)



ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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Specifications & design are subject to change without prior notice.